zorro2

COLLABORATORS			
	TITLE : zorro2		
ACTION	*NAME*	*DATE*	*SIGNATURE*
WRITTEN BY		August 23, 2022	

REVISION HISTORY			
NUMBER	DATE	DESCRIPTION	NAME

Contents

Chapter 1

zorro2

1.1 ZORRO-II

```
                A2000   ZORROII                 Pin             Remark

all data & adresses are buffered


                the authorS

                BUGS
                @{ "GND" link "gnd"}
                1
                @{ "GND" link "gnd"}
                2
                @{ "GND" link "GND"}
                3
                @{ "GND" link "GND"}
                4
                @{ "+5V" link "+5V"}
                5
                @{ "+5V" link "+5V"}
                6
                       ( 470 $\mathrm{\mu}$F to ground 4 )
@{ "_own" link "_own"}
                7
                     (buster, 41)
@{ "-5V" link "-5V"}
                8
                @{ "_slavex" link "_slavex"}
                9
                   (buster, 12+X)
@{ "+12V" link "+12V"}
                10
                @{ "_cfgout" link "_cfgout"}
                11
                @{ "_cfginx" link "_cfginx"}
                12
                  X indicates portnr.
@{ "GND" link "GND"}
                13
```

```
@{ "_c3" link "_c3"}
14
@{ "CDAC" link "CDAC"}
15
@{ "_c1" link "_c1"}
16
@{ "_ovr" link "_ovr"}
17
@{ "XRDY" link "XRDY"}
18
@{ "_int2" link "_int2"}
19
@{ "-12V" link "-12V"}
20
@{ "A5" link "adresswire"}
21
@{ "_int6" link "_int6"}
22
@{ "A6" link "Adresswire"}
23
@{ "A4" link "Adresswire"}
24
@{ "GND" link "GND"}
25
@{ "A3" link "Adresswire"}
26
@{ "A2" link "Adresswire"}
27
@{ "A7" link "Adresswire"}
28
@{ "A1" link "Adresswire"}
29
@{ "A8" link "Adresswire"}
30
@{ "FC0" link "FC"}
31
@{ "A9" link "Adresswire"}
32
@{ "FC1" link "FC"}
33
@{ "A10" link "Adresswire"}
34
@{ "FC2" link "FC"}
35
@{ "A11" link "Adresswire"}
36
@{ "GND" link "GND"}
37
@{ "A12" link "Adresswire"}
38
@{ "A13" link "Adresswire"}
39
@{ "_eint7" link "_eintx"}
40
@{ "A14" link "Adresswire"}
41
@{ "_eint5" link "_eintx"}
```

```
                42
                @{ "A15" link "Adresswire"}
                43
                @{ "_eint4" link "_eintx"}
                44
                @{ "A16" link "Adresswire"}
                45
                @{ "_beer" link "_beer"}
                46
                @{ "A17" link "Adresswire"}
                47
                @{ "_vpa" link "_vpa"}
                48
                @{ "GND" link "GND"}
                49
                @{ "E" link "E"}
                50
                @{ "VMA" link "VMA"}
                51
                @{ "A18" link "Adresswire"}
                52
                @{ "_rst" link "_rst"}
                53
                @{ "A19" link "Adresswire"}
                54
                @{ "_hlt" link "_hlt"}
                55
                @{ "A20" link "Adresswire"}
                56
                @{ "A22" link "Adresswire"}
                57
                @{ "A21" link "Adresswire"}
                58
                @{ "A23" link "Adresswire"}
                59
                @{ "_brx" link "_brx"}
                60
                @{ "GND" link "GND"}
                61
                @{ "_bgack" link "_bgack"}
                62
                @{ "D15" link "Datenwire"}
                63
                @{ "_bgx" link "_bgx"}
                64
                @{ "D14" link "Datenwire"}
                65
                @{ "_dtack" link "_dtack"}
                66
                @{ "D13" link "Datenwire"}
                67
                @{ "READ" link "READ"}
                68
                     (buster,35)
@{ "D12" link "Datenwire"}
                69
                @{ "_lds" link "_lds"}
```

```
                70
                @{ "D11" link "Datenwire"}
                71
                @{ "_uds" link "_uds"}
                72
                @{ "GND" link "GND"}
                73
                @{ "_as" link "_as"}
                74
                @{ "D0" link "Datenwire"}
                75
                @{ "D10" link "Datenwire"}
                76
                @{ "D1" link "Datenwire"}
                77
                @{ "D9" link "Datenwire"}
                78
                @{ "D2" link "Datenwire"}
                79
                @{ "D8" link "Datenwire"}
                80
                @{ "D3" link "Datenwire"}
                81
                @{ "D7" link "Datenwire"}
                82
                @{ "D4" link "Datenwire"}
                83
                @{ "D6" link "Datenwire"}
                84
                @{ "GND" link "GND"}
                85
                @{ "D5" link "Datenwire"}
                86
                @{ "GND" link "GND"}
                87
                @{ "GND" link "GND"}
                88
                @{ "GND" link "GND"}
                89
                @{ "GND" link "GND"}
                90
                @{ "GND" link "GND"}
                91
                @{ "7M" link "7M"}
                92
                        system clock
@{ "DOE" link "DOE"}
                93
                @{ "_busrst" link "_busrst"}
                94
                @{ "_cbg" link "_cbg"}
                95
                @{ "_eintx" link "_eintx"}
                96
                @{ "nc" link "nc"}
                97
                  nc
```

```
@{ "GND" link "GND"}
                99
                @{ "GND" link "GND"}
                100
```

1.2 nc

not used

1.3 gnd

nothing special, just 0V

1.4 +5v

+5 voltage to feed some ic's
2-4 Amperes per slot.

1.5 _own

a line who ends in BUSTER pin 41,
tells the system that the expansioncard controls the dma
all by itself.

1.6 -5v

-5V for special things.
300 mAmpere total.

1.7 _slavex

x is a number from 1-5 and indicates the slot where this
signal occured.

Each slot has its own slave-signal,to prevent bus-errors or
similar fatal things.

Signals system that current slot is in slave mode.

1.8 +12v

```
from the powersurply
8 Ampere total.
```

1.9 _cfgout

```
for the autoconfig its mixed with _copcfg from MMU-port via
a chain of 74LS32.
  Used for Autoconfig.

notice: the slots of the amiga are have fixed priority,
  beginning with the 86 pin slot (highest)
     ending with the 100p slot (lowest)
```

1.10 _cfginx

```
x is a number from 1-5 and indicates the slot where this
signal occured. Used for Autoconfig.
```

1.11 _c3

```
                an other
              clock
                Its a _c1 but moved by 1/2 ¶ (90 degrees)

7M      11110000111100001111100001111
CDAC    11000011110000111110000111100
```

1.12 cdac

```
                a 7M
              clock
               but moved 1/2 ¶ (90 degrees)

7M      11110000111100001111100001111
CDAC    11000011110000111110000111100
```

1.13 _c1

```
                3.58 MHz = 7M /2 + ¶/2 (90 degrees)
              clock
                7M      11110000111100001111100001111
c1      00001111111100000000011111111
```

1.14 7m

```
                system
              clock
               NTSC and PAL have a little bit
different speed.

PAL     7.16 Mhz
NTSC    ?    Mhz
```

1.15 _dtack

```
  Data transfer acknowledged.

  Signals succesfull datatransfer from the slots to the 680x0.
```

1.16 _ovr

```
this is one of GARY's pins (29).
Used for Autoconfig.
used to shut of internal generation of _dtack.not usable
in ranges from $200000 to $9fffff
```

1.17 xrdy

```
this is one of GARY's pins (31).
Used for Autoconfig.
external ready,used to delay the _dtack generated by the system.
```

1.18 _int6

```
Connected to Paula,causes Level 6 Interrupt.
```

1.19 _int2

```
Its connected to PAULA. causes an interrupt 2.
```

1.20 _eintx

```
x=1,4,5,7
runs trough a 74ls08 (inverter,U802) then to 74ls148
(demultiplexer,U804) and ends in _IPLx.

notice: these are the decoded iplx singals from the 86-pin bus.
```

1.21 -12v

```
    from powersurply
    300 mAmperes total
```

1.22 _cbr

```
BUSTERstuff pin 28
```

1.23 _cbg

```
BUSTERstuff pin 27
```

1.24 doe

```
BUSTERstuff pin 47
DataOutEnable enables the buffers for the databus
```

1.25 _busrst

```
buffered reset for peripherie
```

1.26 ipl

```
three interrupt-inputs of the 680x0.
are decoded to 7 priority-levels.
```

1.27 fc

```
function code lines, all driven by a 74ls245 (U605)
signals the hardware on which data or pogram-area
is currently accessed.used by mmu.
```

1.28 _as

```
adress-strobe, is driven by a 74ls245 (U605)
signal on low that the data on the adress-bus is valid.
```

1.29 _beer

```
buserror
access while normal cycle on illegal address.
```

1.30 _bgx

```
busgrant
something signals that it need access to the bus.
the cpu signals something that it now may access the bus.
```

1.31 _bgack

```
busgrant acknowlegde
the cpu signals something that it now may access the bus.
bgack is used to acknowledge that the bus has been granted.
```

1.32 _brx

```
x indicates which slot
busrequest
something signals that it need access to the bus.
```

1.33 _lds

```
lower data strobe, is driven by a 74ls245 (U605)
signals access on lower bus (D0-D7)
```

1.34 _rst

```
reset, but beware power-up reset isnt just _rst !
```

1.35 read

```
this line is r/w,is driven by a 74ls245 (U605)
bus is been read on high.
```

1.36 _uds

```
_upper data strobe, is driven by a 74ls245 (U605)
singals access on upper bus (D8-D15)
```

1.37 vma

```
valid memory adress
signals that the mc680x0 has synchronized to the e-signal
and the current adress on bus is valid.
```

1.38 _vpa

```
valid peripherial adress
used to synchronize datatransfer via e-signal.
if low,current adress on bus is valid.
```

1.39 adresswire

```
One of the processor adresslines. all lines of adress&data-bus
are driven by a couple of 74LS245 (U600/601/602).
```

1.40 datenwire

```
One of the processor datalines. all lines of adress&data-bus
are driven by a couple of 74LS245 (U603/604).
```

1.41 unknown

```
no idea what happens here. nc,gnd or what ?
```

1.42 _hlt

```
  if low,the 680x0 is temporarily stopped at the end of the current buscycle.
```

1.43 e

```
It's a special feather of the 68000. Its 1/10th of the systemclock.
You may need it to syncronize with other peripherie.
```

1.44 clock

```
28M   10101010101010101010101010101010101010101010  base for all purposes

CDAC  11110000111100001111000011110000111100000  7.16 MHz
_c1   00111111110000000011111111100000000111111  3.58 MHz
_c3   11111100000000111111110000000011111111100  3.58 MHz
 7M   11000011110000111100001111000011110000011  7.16 MHz
CCK   11000000001111111100000000111111111000000  3.58 MHz
CCKQ  00000011111111000000001111111110000001111  3.58 MHz

E is a special from the 68000. Its 1/10th of the systemclock.

!_c1 = CCK
!_c3 = CCKQ

     REPLACE WITH PICTURE
```

1.45 autor

```
A guy who didnt find the zorro description. had to figure out
by myself so i made the ascii file, but that wasnt nice.
My english ? ups, i am not english so NO COMMENT :)
The idea is to make more such files about AGNUS, GARY ,....
than we will have a big database for all people hacking on
the AMIGA. If you contibute too, remove errors (note in BUGS!)
and write a bit soon we will have the first computer database
for AMIGA, entire in PD.

your    A1000

Updated on 8.1.1996 by MNT. Just another guy that repairs
about 5 amigas a day.
contact: http://www.FH-Karlsruhe.de/~fema0012/
```

1.46 bugs

```
BUGREPORT

DATE:   what changed , who changed

this file should not exceed 40 lines

8.1.96  Several signals explaned,
  unknown signals updated,
  several wrong pins changed. (MNT)
```